Point to Point Microwave Communication with Gigabit Throughput

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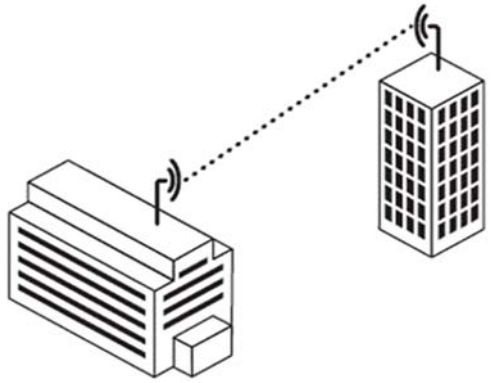
Abstract

More and more there is a need to connect remote locations to the internet and the only feasible way of doing so is with a reliable high throughput wireless link. There is currently a lack in reliable products to complete this important task. This is a proposal for students to develop such a wireless communication link and turn it into a product that could be marketed. This project would use many existing technologies to form a reliable product that can be manufactured for a reasonable price and still meet the demands of corporate networks.

By working on this project the members of the team will learn valuable skills about high speed communication, circuit design and FPGA implementation. They will grow their knowledge and have a great product that they can use to demonstrate their real world skills making them much more hirable.

Project Description

The entire world is connected by cables and wires that make up the internet as we know it today. However, as we begin to add more and more remote locations to the internet, it is infeasible to bring a physical cable to them. This need has spawned wireless internet, a major contributing factor in connecting remote locations to the internet. However, there are limitations to Wi-Fi, including range and speed. Developing a 10 GHz wireless link will help to solve problems with remote internet access by providing high speed wireless communication at a reasonable distance. We believe that we can achieve a link of 1GbS, which is as fast as most wired commercial systems. This system will be composed of two parts: an Analog front end to generate and receive the signals, which will interface to a high speed digital backend that will communicate over traditional Ethernet for compatibility with existing technologies. The design of these two parts will have to happen in concert to ensure that they can work together and exist in close enough proximity to become a functional product.



Example use of a high-speed point to point link like the one proposed herein.

Antenna and Waveguide

To more completely explain the project, we have broken it down into functional blocks. The first, and perhaps most complex part of the project will be receiving the RF signal and turning it into a usable electrical signal. This process is handled by the antenna. Because communication is happening between two stationary locations, directional antennas will be used. At 10GHz the best directional antenna will either be a horn or patch antenna [1]. Once the signal has gone through the antenna, it will need to be transferred to the next stage through a waveguide. The use of a quarter wave stub to cancel out any harmonics will allow for a smooth and efficient transfer of the signal and is known as impedance matching [2]. By using this technique any high frequency noise or harmonics can be filtered out [3]. These concepts are fairly well developed for things in the 10GHz band because it is used for HAM [4].

Frequency Mixer

Once the signal has been slightly conditioned and transferred into an electrical signal, it needs to be converted into a lower, more usable frequency. This process is called “beating it down,” and is performed by a frequency mixer [5]. The mixer takes in the RF signal and a known, locally-generated, frequency from the local oscillator and generates the mathematical difference of the two frequencies. [6]. This IF can then be more easily transmitted around the circuit, and can be better handled by the rest of the demodulation circuitry [4].

Phase Locked Loop

The intermediate frequency can be fed into a circuit element called a PLL, which compares the phase of a controllable local signal to the received signal. Because it uses a voltage to control the oscillator, the control voltage is proportional to how far the received signal is from the center or carrier frequency [7]. In a frequency modulation schema, similar to the one proposed for this project, this control voltage is effectively the information that that is being transmitted. The actual proposed modulation schema is a subset of frequency modulation know as frequency shift keying; the difference is that true FM transmits an analog signal by moving continuously across a set of frequencies, whereas FSK jumps between two discrete frequencies that represent two binary values [2].

Field Programmable Gate Array

The voltage value that is generated from the phase locked loop will be passed to FPGA through a simple comparator that will clean up the signal from the slightly noisy PLL. Once the signal is in the FPGA, it can be processed through the complex and programmable logic [8]. The data will be transmitted in packets that include a parity bit. The reason for using these packets is that the FPGA will need to deconstruct the packet, perform the error correction, and then reconstruct the data into Ethernet packets [9]. The FPGA is controlled by a software program that will be developed as part of this project. Also, the FPGA will require special considerations for power management and layout, including a number of tightly controlled power rails. The sampling rate of the FPGA will dictate the speed at which we can send and receive bits, and therefore the throughput.

Error correction

By including a special bit in each packet that is procedurally generated based on the contents of the packet, any bits that are lost or corrupted can be recreated [9]. This process is known as parity and is quite robust against single bit loss, while not requiring significant overhead. However, if we find that there is more loss in our system that cannot be eliminated otherwise, we may have to increase the number of parity bits we use, thereby increasing the overhead and possibly limiting our throughput.

Plan of Work

The project can be broken down into three pieces: research, spin 1 and spin 2. The phrase “spin” is used because each one will involve a complete overhaul of the project and is a common practice in industry. The full project schedule is included in appendix A as a Gantt chart. The first stage has already commenced and provided this proposal is approved will continue into the summer. Both team members will be working full time at internships during the summer but research will continue. These internships themselves will actually assist in the background research process as they will give the team members the chance to get exposure to many of the concepts included in this project.

Starting in the fall semester of 2015 the project will go into full swing, with both members putting in an excess of 20 hours a week on spin 1. Because of the clear divide between the RF and digital parts of the project, it should be easy for the members to work in parallel without many dependencies on the others progress. One member will start by working on the beginnings of the FPGA code, developing an Ethernet stack to capture packets transmitted to the device from the Ethernet port. The other member will be working on circuit design, starting with the PLL and moving onto the frequency mixer. From there, the digital team member can move onto developing a robust error correction strategy; while the other member starts on the antenna and waveguide design. There are a number of milestone dates set out on the Gantt chart where all stakeholders will be brought together to assess progress and evaluate any deliverables. Spin 1 will come to a culmination in the final weeks of the semester with all members working to get any final problems worked out in time for a demo at the end of the semester.

Spin 2 will commence with the beginning of the spring 2016 semester. This time through the emphasis will be more on optimization of the project for manufacturability, marketability and cost. Few if any additional features will be added but the intent is to turn the project from something that works once in the lab into something that could be manufactured and deployed in the real world. Again, there will be stakeholder meetings throughout the semester to evaluate progress and deliverables. The second spin may also spawn the need to bring in a legal team to evaluate the project for patentability. At the end of the semester there will be another presentation with the final product.

People

The two individuals that will comprise the development team are Thomas Murphy and Zach Hudson. Murphy is a computer engineering student and will work on developing the FPGA code. He has prior experience with a hardware design internship previously and will be going to National Instruments for summer 2015 where he will be working with their signal conditioning group. This internship especially will solidify his working knowledge with the digital signal processing required to make this project a reality. Hudson is an electrical engineering major specializing in analog circuit design. He has two prior hardware design internships where he has gained significant knowledge in circuit board design and layout. In the summer of 2015 Hudson will be going to Motorola Solutions and working with their applied technology department gaining experience in telecommunications and RF design. With this combination of backgrounds they will make a powerful team to tackle this challenge and have enough experience with developing marketable products.

We are requesting the assistance of electrical engineering professor Dr. Frank Merat and lab director and PhD candidate Ed Burwell. Each of these men brings a specific set of skills to this project and will be perfect mentors and evaluator. Dr. Merat has extensive experience as a researcher in the area of analog circuits and communication theory. Mr. Burwell has exceptional experience with high frequency applications and with FPGA design. It is our belief that both of these individuals will see the merits of this project for the team members' educations and a potentially viable product.

Budget

The product development nature of this project means that traditionally, the largest cost would be the engineering time. Because it will be completed as part of the curriculum for senior project the engineering time will not have a direct cost associated with it. The other costs will primarily be for materials. Below is a projected budget broken out by spin:

Spin 1	Cost per	Qty	Cost
Arria V GX Starter Kit	$ 850.00	2	$ 1,700.00
Arria V to RF Frontend Cables	$ 100.00	2	$ 200.00
RF Frontend PCB Manufacturing	$ 150.00	4	$ 600.00
RF Frontend Bill of Materials	$ 75.00	4	$ 300.00
Antenna Materials and Cables	$ 50.00	2	$ 100.00
	Spin 1 Total		$ 2,900.00
Spin 2			
Arria V GX Starter Kit	$ 850.00	Reuse	$ -
Arria V to RF Frontend Cables	$ 100.00	Reuse	$ -
RF Frontend PCB Manufacturing	$ 150.00	3	$ 450.00
RF Frontend Bill of Materials	$ 50.00	3	$ 150.00
Antenna Materials and Cables	$ 25.00	2	$ 50.00
	Spin 2 Total		$ 650.00
	Project Total		$ 3,550.00

The Arria V and its cable harness can be reused for the second spin because we will not be changing anything about the physical board. The RF frontend board and antenna assembly will be redesigned as part of the second spin and new ones will need to be fabricated from the new design files. The funding for this project will be sourced from a number of places. The primary source of funding will be corporate sponsors. Having companies willing to donate products or money to the project is the only way that it will be funded. As such we will be offering companies incentives for sponsoring including having their name associated with any publication or promotional material. The disparity between the fundraised total and actual cost will need to be covered by other means and we are looking into other options including ThinkBox, EECS department, or HackSoc funding.

References

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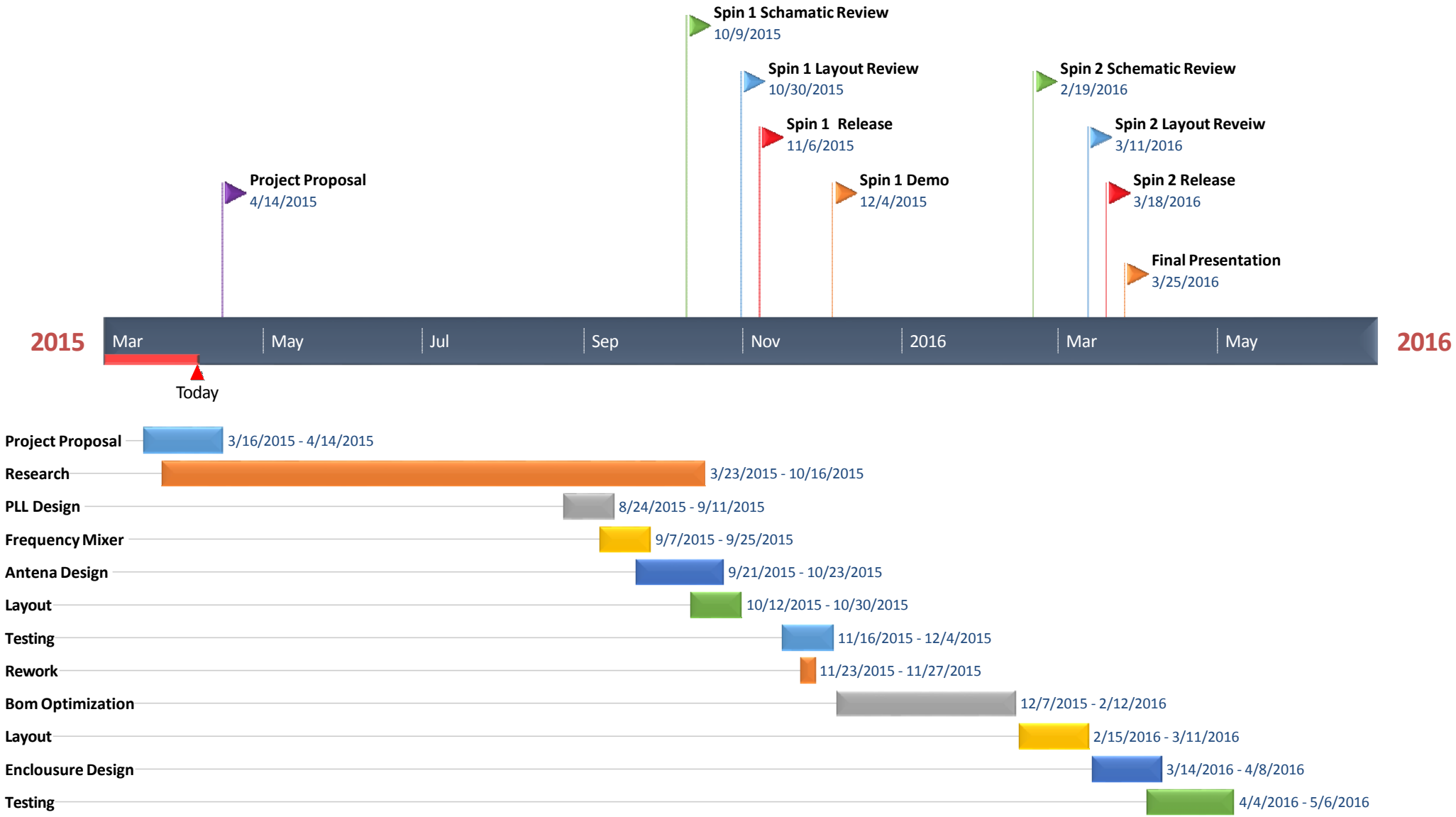
Appendix A: Gantt Chart



Appendix B: Glossary of Terms

Note: Because the primary audience is familiar with the technical jargon used, it would be inappropriate to define all term. Below I have provided a brief glossary of terms that an unfamiliar reader may need to know before the proposal can be completely understood.

HacSoc: EECS student group that encompasses the IEEE and ACM groups as well as providing other services including a hardware lending library, tech talks, annual conference and annual Hackathon.

IEEE: Institute of Electrical and Electronics Engineers, professional organization for electrical and computer engineers and related fields.

ACM: Association of Computer Machinery, professional organization for computer science and related fields.

GHz: Gigahertz

GbS: Gigabits per second

HAM: amateur radio as defined by the FCC

FCC: Federal Communications Commission

PLL: Phase Locked Loop

IF: Intermediate Frequency generated by the “beat down” process.

FSK: Frequency Shift Keying, a modulation schema that uses two discreet frequencies to encode binary data

FPGA: Field Programmable Gate Array