Microwave Digital Communication Radio

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Executive Summary

The goal of this project is to develop the first step to create a marketable product for wireless backhaul communication. This first stage of the development will be limited in scope to creating a proof of concept transceiver capable of creating and recording digitally modulated I and Q data. Future development is planned to implement a monolithic transceiver board and the appropriate antennas for a final working demonstration system. The target for the fall semester EECS 398 is to complete the first stage. This stage will be composed of the development of the transceiver board and support circuitry for integration with a purchased FPGA development board. The deliverables for this semester will be the transceiver board, populated and tested, with the corresponding interface development for the FPGA. As a final demonstration we plan to be able to transmit I and Q data and, by building two transceivers, we should be able to recreate the data on the other side. The total cost for this project is projected at $2765 but our intent is to have corporate sponsorship that should make the out of pocket expenses negligible.

Background

A core component of wireless communication is high-bandwidth communication between high-throughput nodes. When the resources are available, high reliability communication can be achieved through direct connections through cable or fiber optic lines. However, these connections have a high initial cost, fixed layout, and require space for the physical placement. These disadvantages can be overcome by using wireless backhaul links. These are generally point-to-point data connections that use higher frequency radio bands that are less occupied by existing technologies.

To allow sufficient flexibility of the communication system, most of these communication systems are controlled by a field-programmable gate array (FPGA). This allows extensive and reconfigurable algorithms to be used depending on the requirements of the specific installation. For these dedicated point-to-point systems, the communication implementation can be significantly less complicated than the requirements of point-to-multipoint or multipoint-to-multipoint communication of current and future mobile networks.

In addition to configurable signal processing, the front-end signal path must be sufficiently configurable to meet the radio band diversity and regulatory compliance. This will become a larger issue going forward as creating a marketable product will entail full compliance with relevant regulations including FCC part 15.

Project Objectives

The objective of this project is to create the transceiver board and FPGA intellectual property components for transmission of quadrature amplitude modulated data. The project will be limited in scope to only generating I and Q data with plans for future development of the RF frontend. We will be using an FPGA development board and building our own board for the QAM transceiver with all of the supporting electrical components and filters.

The FPGA will handle communication between the source of digital data and high speed data converters. This includes handling the majority of the digital signal processing, encoding/decoding the information for use in the radio communication channel, and managing the state of the support circuitry. Prior to the development of the complete system, the FPGA will be used to verify the communication interfaces with the data converter and the performance of the transceiver board.

The transceiver board will be built around the Texas Instruments AFE7225 Dual 12-Bit, 125MSPS ADC with dual 12-Bit, 250 MSPS DAC which will do direct synthesization of the I and Q data outputs based on the LVDS inputs after applying some digital filtering. Additional analog filtering will need to be provided for the I and Q data stream before they can be broken out to the connectors for further upconversion on the later digital board.

Project Milestones

The nature of building a large tightly integrated system such as this limits the ability to use agile or spiral development models however there are tangible milestones that can be laid out and used to judge progress. These milestones are below:

Hardware Components

1. Block diagram
2. Component and architecture selection
3. Support circuitry determination
4. Schematic design
5. Component placement and signal planning
6. Layout and routing
7. Board manufacture
8. Board population and testing

Software Components

1. Digital interface specification (in parallel with component selection)
2. Configuration interface implementation

3. Data interface implementation
4. Signal generation for test
5. Communication to a host computer for verification and control

Budget

Much of this project is made up of expensive high end parts and services. This is the cost of doing business on the cutting edge of communications systems and it is too much for any senior project group to bear themselves. We will be reaching out to many of the companies that either create the components that we need,frequently use them in their own projects looking for sponsorships, or manufacture similar designs for large customers. This will help to offset the costs and keep our total out of pocket expenses reasonable.

Item	Cost per	Quantity	Line Total
FPGA	$850	2	$1700
Transceivers	$55	3	$165
Other Components (per Board)	$100	3	$300
PCB	$200	3	$600
		Total	$2765